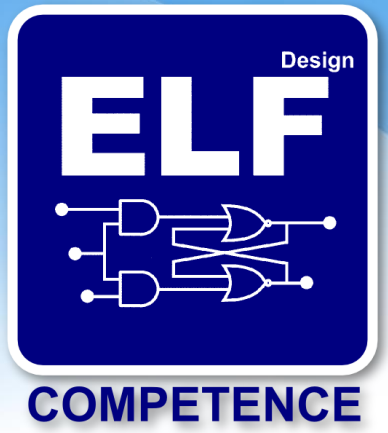


ASML

From High-Level Algorithms to ASML Automated Digital Design Flows

John van Tol
Competence Leader Embedded Logic and Firmware (ELF) Development

May 21st, 2019 - Eindhoven

Key Takeaways

1. ASML business drivers: Quality and Time-to-Market, require an efficient workflow for getting smart algorithms into high speed digital hardware (FPGAs)

2. Adoption of Model-Based Design into the ASML Digital Design Flow achieves this with automatic generation of HDL source code and test bench code

3. Model-Based Design reduces the gap between system architect and design engineer

MAKE IT WORTH IT

MAKE US GROW

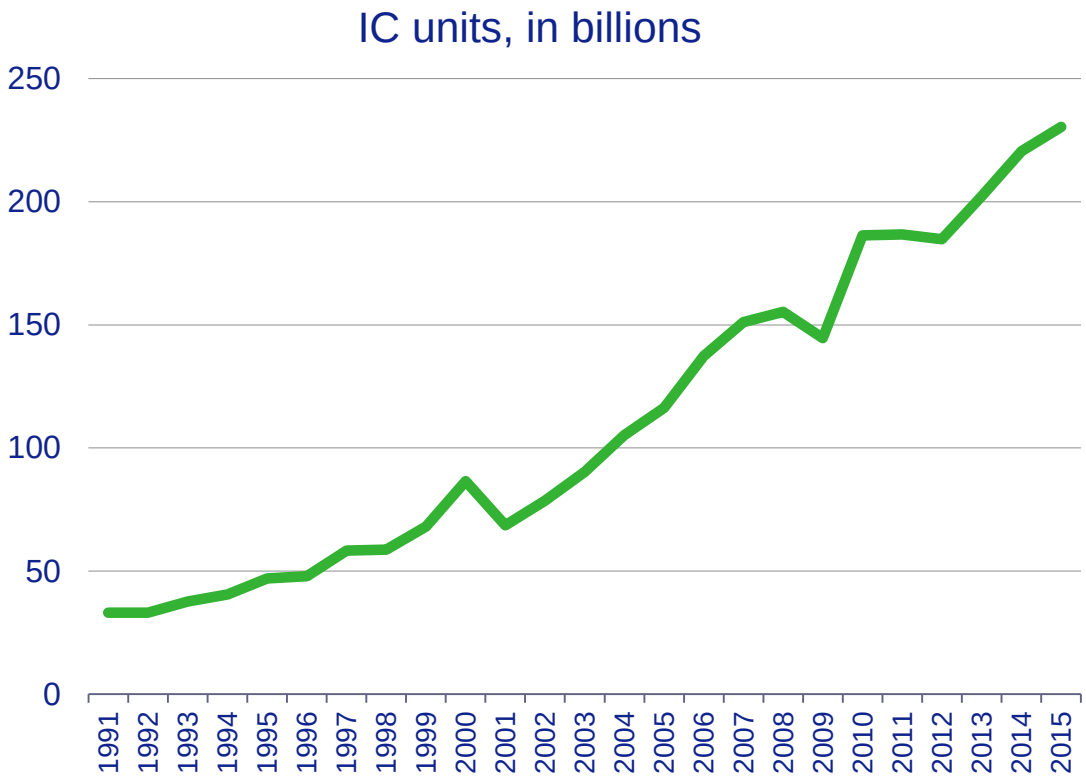
MAKE IT TOGETHER

MAKE IT WORK

MAKE IT WELL

Chips are everywhere!

In 2015, 230 billion ICs were made, 30 for every man, woman and child on the planet



Semiconductor Revenue Milestones	
$50B	1989
$100B	1994
$200B	2000
$300B	2010
$400B	2017
$500B	2019

Data: WSTS

We develop and build lithography systems for manufacturing those IC's

150 tons of precision equipment

works with single nano-meter precision:

Grass grows at a speed of 33 nano-meter per second

Moore’s Law means doing “More with Less”

Cray Super Computer
1976

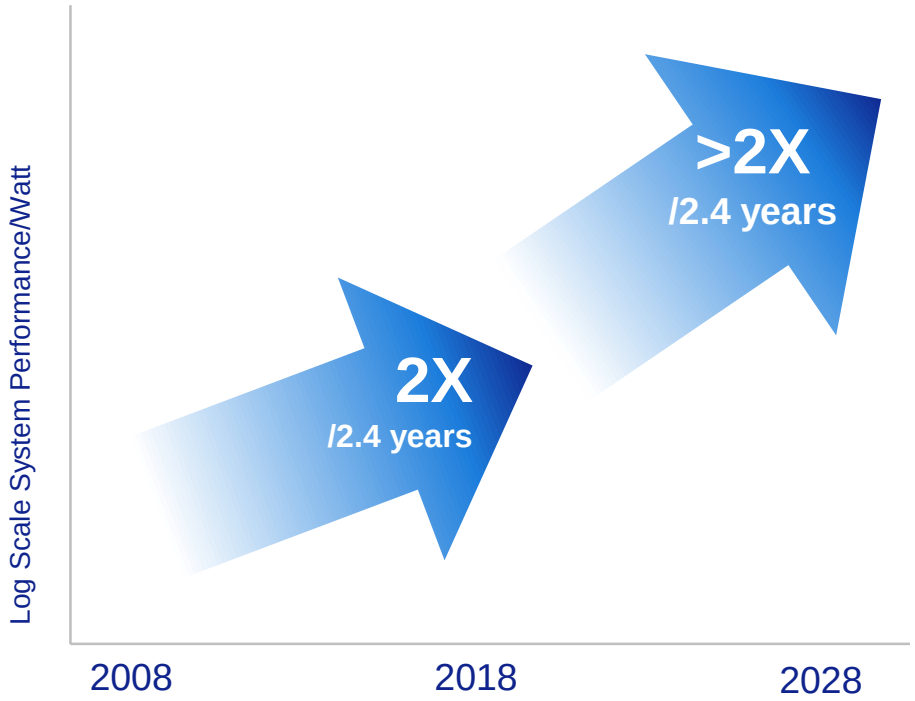
30M$, 8 Mb, 5500 kg, 150 kW

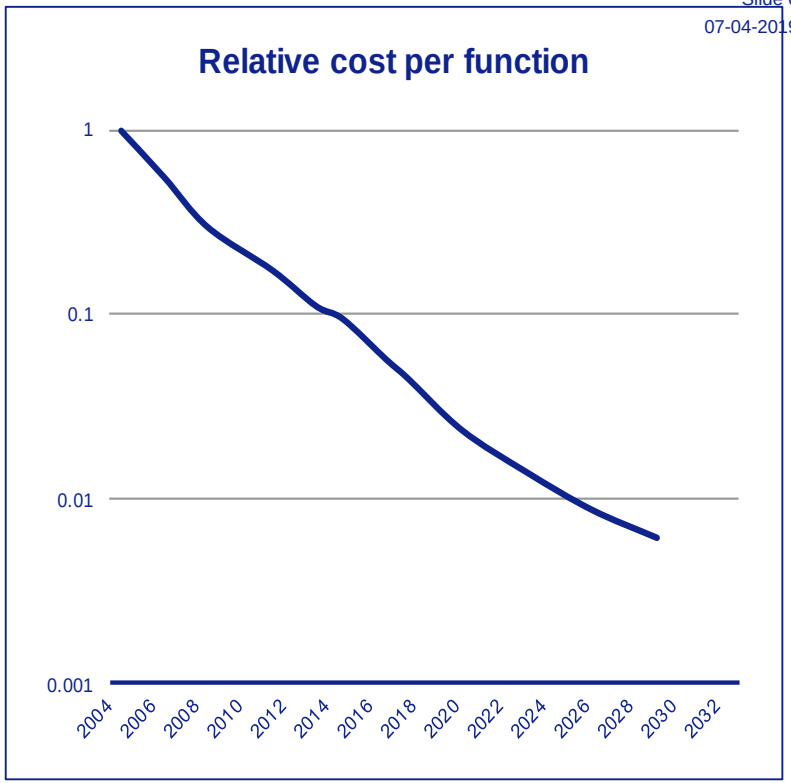
2018

1000 $, 512 MB + GB flash, 200 g,< 1W

The industry is driven by Moore's law,

which continues, through ideas and value creation

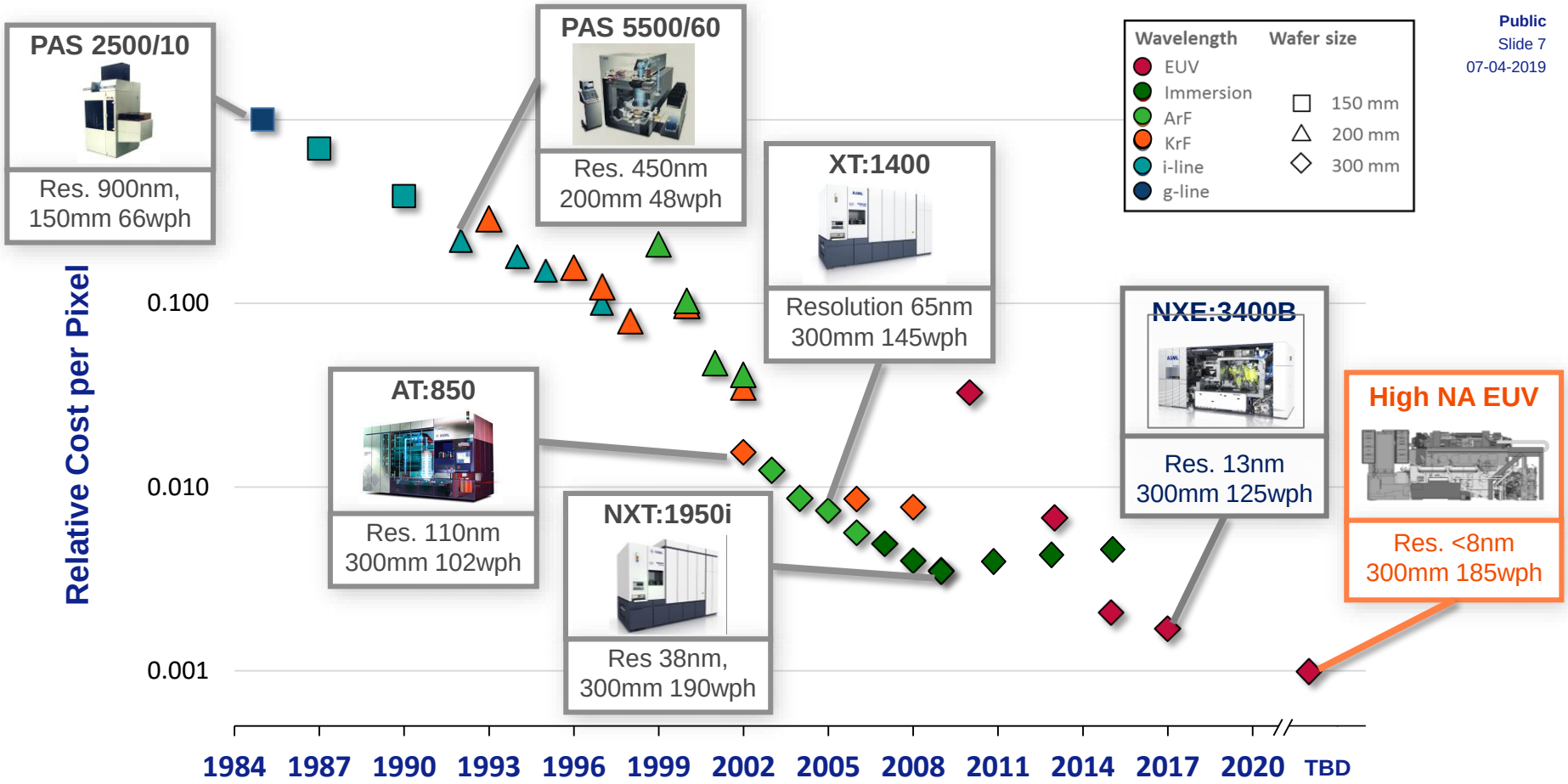




This is what we're doing it for!

[1]Lisa Su, AMD, "Immersive era in consumer computing", IEDM, dec 2017
[2]Gordon Moore, "Progress in digital integrated Electronics" International; Electronic Device Meeting,, IEEE, 1975, p p 11-13
ASML Market Research

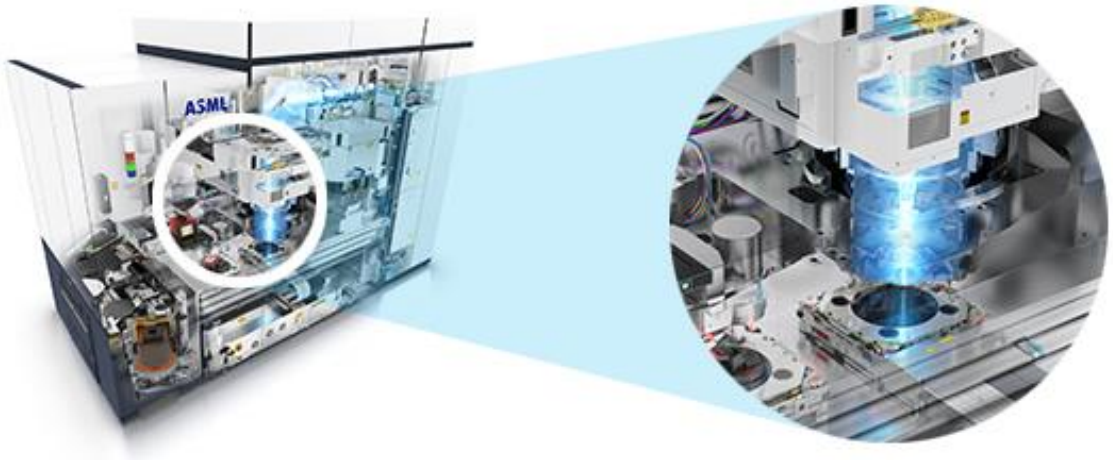
Our systems enable the faster, better, cheaper chips of tomorrow



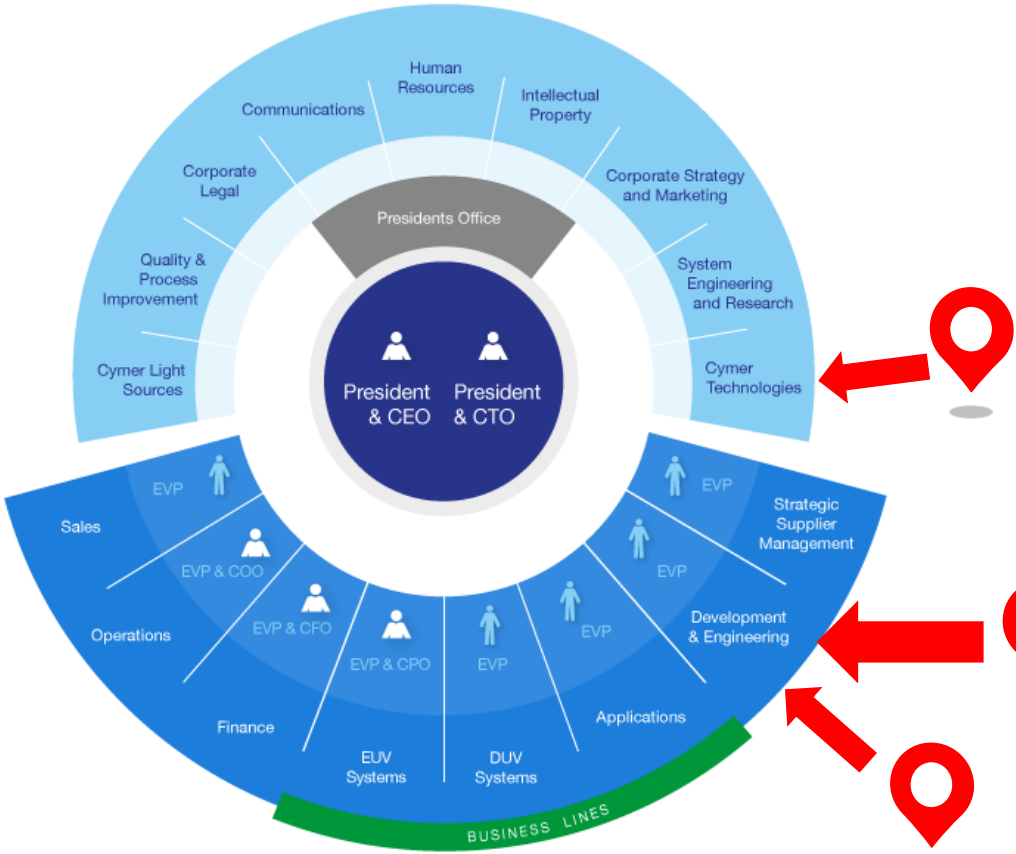
Source: ASML Product specs, Market Research

ASML makes the machines for making IC's

Resolution:	>1μm	> 500 nm	> 400 to 90 nm	> 100 to 38 nm	> 32 to16 nm
Overlay:	250 nm	100 nm	100 to 12 nm	20 to 4 nm	2 nm



Electronic Development within D&E ASML



ELF Design COMPETENCE

Embedded Logic Firmware

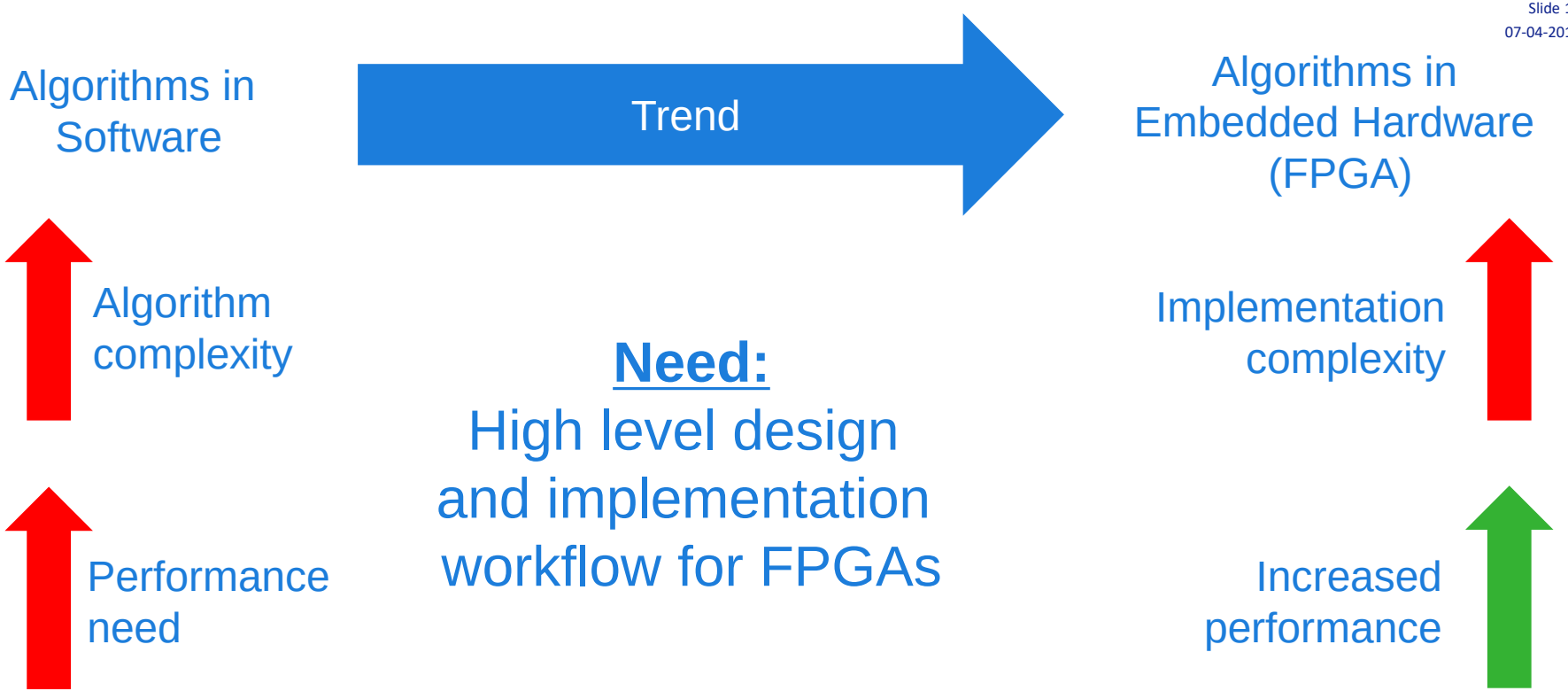
EDEV San Diego USA

EDEV Veldhoven The Netherland

EDEV Wilton USA

Goals and Challenges

Challenges



Need:
High level design and implementation workflow for FPGAs

MAKE IT WORTH IT
MAKE US GROW
MAKE IT TOGETHER
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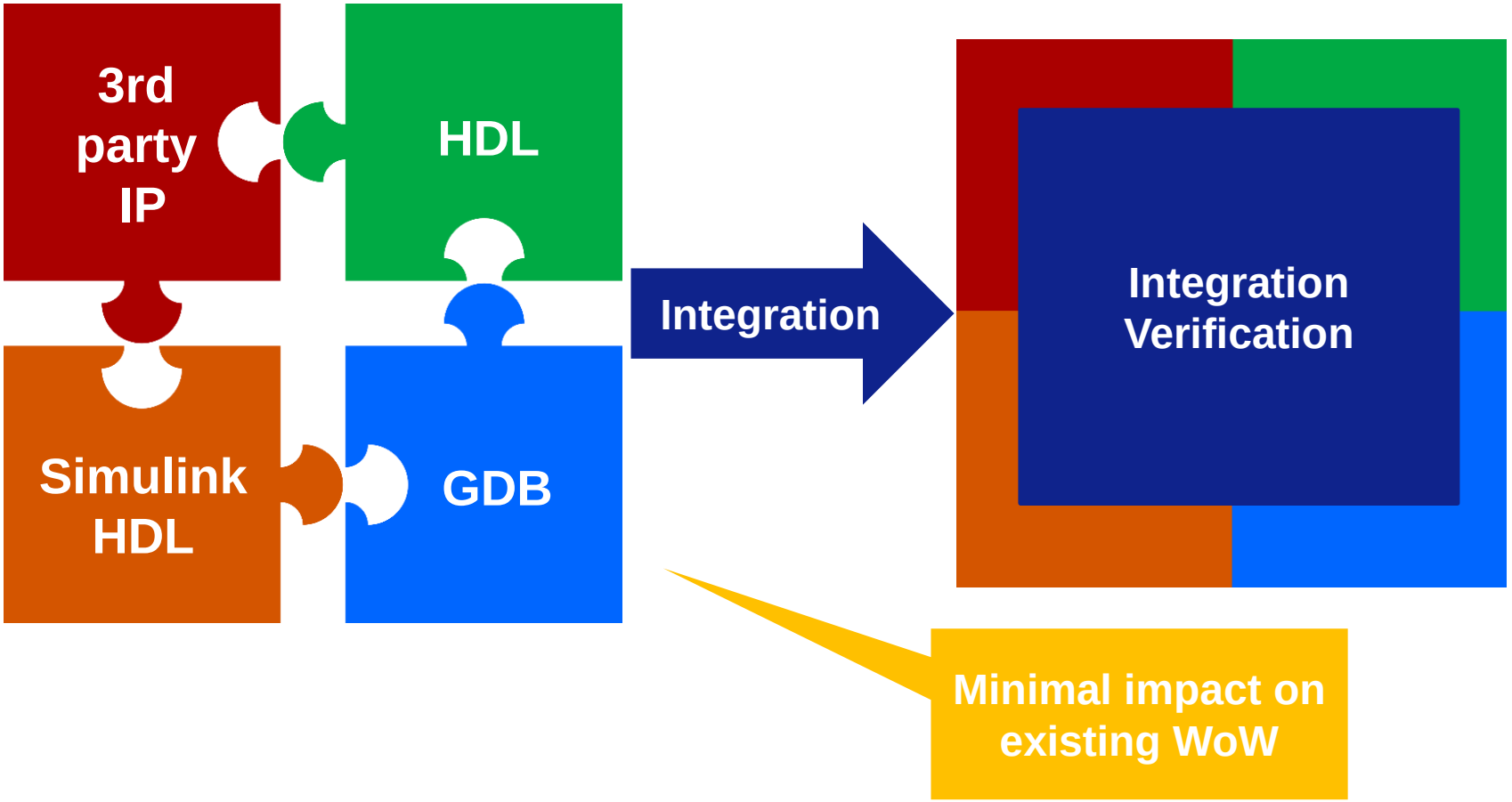
MAKE IT WELL

Goals

1. One ASML common method of developing algorithms in FPGAs
2. Make modeling, simulation and code generation accessible for ELF engineer
3. Reduce the gap between system architect and ELF engineer

How we do it

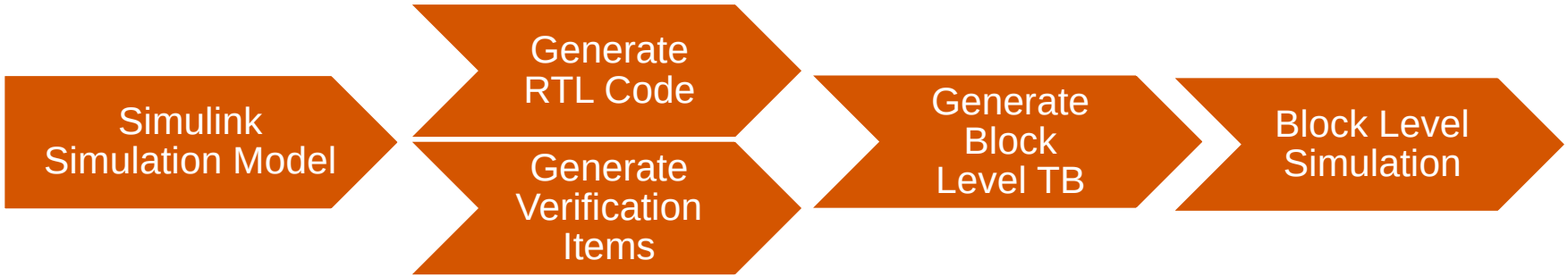
ASML ELF Way-of-Working (WoW)



GDB = Generic Design Block, HDL = Hardware Description Language

ASML ELF Way-of-Working, elaborated

Simulink HDL



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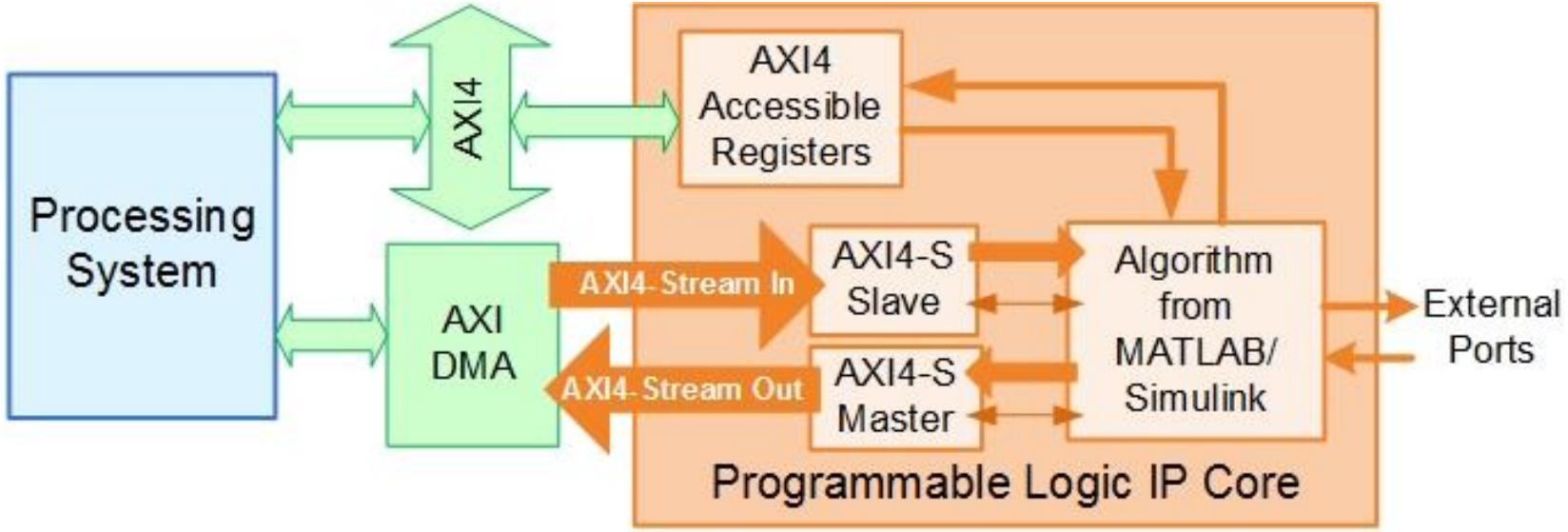
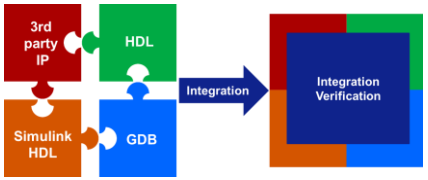
ASML workflow to create algorithm subsystem, an example



Automated Build and Test



Design → Compilation and Simulation → System generation (PlatformDesigner, XPS, Vivado) → Synthesis and place and route

1. Buildfiles are used to automate the various tasks involved in the FPGA design flow

2. The “Build process” makes extensive use of (GNU) Make

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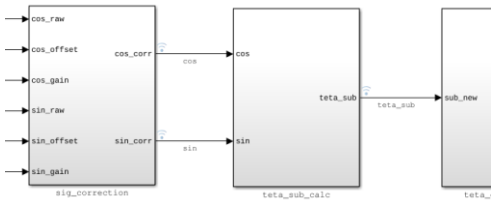
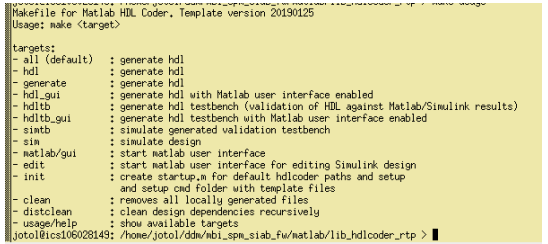
Achievements and Outlook

Using HDL Coder in ELF projects

- **Established workflow within the entire ASML organization.**
  - IT team (IT4E) maintains development software and Linux servers for any ELF project
  - Standard use of HDL Code Generation in ELF Design Flow (DDM2/Buildfiles)
  - Integrated with workflow for communication protocols (GDB), integration tool (QSYS/Platform designer/Vivado Block design), hardware interfaces (VHDL)





- **Improved development of Digital Signal Processing (DSP) functions (vs. handwritten RTL and/or Testbench)**
  - Easier to make changes in a late stage of the project without compromising quality
  - Especially suited for complex DSP functions

- **Future work: automatic FPGA-In-the-Loop (FIL)**

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